higher input-output isolation. The structure could be extended to larger dimensions for high voltage applications at lower frequencies.

[0070] Although the present invention has been described in considerable detail with reference to certain preferred configurations thereof, other versions are possible. The field plate arrangement can be used in many different devices. The field plates can also have many different shapes and can be connected to the source contact in many different ways. For example, the field plate can extend from over the HEMT's active area such that the connection is continuous between the field plate and source contact, instead of through buses or conductive paths. This arrangement can, however, introduce prohibitive capacitance into the structure. Accordingly, the spirit and scope of the invention should not be limited to the preferred versions of the invention described above.

We claim:

1. A transistor, comprising:

an active region having a channel layer;

source and drain electrodes in contact with said active region;

a gate between said source and drain electrodes and in contact with said active region;

a spacer layer on at least part of the surface of said active region between said gate and said drain electrode and between said gate and said source electrode;

a field plate on said spacer layer and extending on said spacer and over said active region toward said drain electrode, and extending on said spacer layer over said active region and toward said source electrode; and

at least one conductive path electrically connecting said field plate to said source electrode or said gate.

2. The transistor of claim 1, wherein said field plate extends on said spacer layer a distance L_{fd} from the edge of said gate toward said drain electrode.

3. The transistor of claim 1, wherein said field plate extends on said spacer layer a distance L_{fs} from the edge of said gate toward said source electrode.

4. The transistor of claim 1, wherein said spacer layer covers said gate and said field plate overlaps said gate and extends on said spacer toward said drain electrode and extends on said spacer layer toward said source electrode.

5. The transistor of claim 1, wherein said at least one conductive path runs between said field plate and source electrode, each said path running outside of said active region and providing said field plate electrical connection with said source electrode.

6. The transistor of claim 1, wherein said at least one conductive path runs between said field plate and source electrode over said spacer layer.

7. The transistor of claim 1, wherein said at least one conductive path runs between said field plate and gate, each said path running outside of said active region and providing said field plate electrical connection with said gate.

8. The transistor of claim 1, wherein said at least one conductive path comprises conductive vias running between said field plate and said gate through said spacer layer.

9. The transistor of claim 1, wherein said spacer layer covers at least part of the surface of said active region from said gate to said drain electrode, and from said gate to said source electrode, said field plate formed integral to said gate and extending on said spacer layer toward said source electrode and said drain electrode.

10. The transistor of claim 1, wherein said plurality of active region is formed on a substrate.

11. The transistor of claim 1, wherein said plurality of active region is formed of Group-III nitride based semiconductor materials.

12. The transistor of claim 1, wherein said spacer layer comprises a dielectric material, or multiple layers of dielectric material.

13. The transistor of claim 1, wherein said gate is at least partially recessed in said active region.

14. The transistor of claim 1, wherein said field plate reduces the peak operating electric field in said HEMT on the drain side of said gate and the source side of said gate.

15. The transistor of claim 14, wherein said reduction in peak operating electric field increases the breakdown voltage of said transistor.

16. The transistor of claim 14, wherein said reduction in peak operating electric field reduces trapping in said HEMT.

17. The transistor of claim 14, wherein said reduction in peak operating electric field reduces leakage currents in said transistor.

18. The transistor of claim 1, comprising a high electron mobility transistor (HEMT).

19. The transistor of claim 1, comprising a field effect transistor.

20. The transistor of claim 1, further comprising one or more spacer layers and field plate pairs, each spacer layer in said pairs providing electric separation between its field plate and the field plate below, each field plate in said pairs electrically connected to said source electrode or said gate.

21. The transistor of claim 1, wherein said field plate comprises separate source and drain field plates said source field plate extending on said spacer layer toward said source electrode and said drain field plate extending on said spacer layer toward said drain electrode, said source and drain field plates electrically connected to said source electrode or said gate.

22. The transistor of claim 1, wherein said field plate comprises separate source and drain field plates said source field plate extending on said spacer layer toward said source electrode and said drain field plate extending on said spacer layer toward said drain electrode, said source field plate electrically connected to one of said source electrode and said gate, said drain field plate connected to the other of said source electrode and said gate.

23. A high electron mobility transistor (HEMT), comprising:

a buffer layer and barrier layer arranged successively on a substrate;

a two dimensional electron gas (2DEG) channel layer at the heterointerface between said buffer layer and said barrier layer;

a source and a drain electrode both making contact with said 2DEG;

a gate on said barrier layer between said source and drain electrodes;